CLAIMS

1. An electronic circuit, comprising:

a semiconductor substrate;

a first layer in a fixed physical relation to the semiconductor substrate;

a well formed in the first layer, wherein the well comprises a first conductivity type and has a side dimension and a bottom dimension;

a first enclosure surrounding the side dimension and the bottom dimension of the well, wherein the first enclosure comprises a second conductivity type complementary of the first conductivity type and has a side dimension and a bottom dimension; and

a second enclosure surrounding the side dimension and the bottom dimension of the first enclosure, wherein the second enclosure comprises the first conductivity type.

2. The electronic circuit of claim 1:

wherein the well comprises a first well; and

wherein the first enclosure comprises:

a second well surrounding the side dimension of the first well; and

a buried layer adjacent the bottom dimension of the first well.

3. The electronic circuit of claim 2 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

4. The electronic circuit of claim 2:

wherein the buried layer comprises a first buried layer; and

wherein the second enclosure comprises:

a third well surrounding a side dimension of the second well; and

a second buried layer adjacent a bottom dimension of the first buried layer.

5. The electronic circuit of claim 4:
wherein the first layer comprises an epitaxial layer; and
wherein the first and second buried layers are formed in the substrate.

6. The electronic circuit of claim 5:
wherein the second and third wells are formed in the epitaxial layer.

7. The electronic circuit of claim 6 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

8. The electronic circuit of claim 6:
wherein the first well comprises circuitry operable to emit electrical holes in response to an operating voltage that may swing between a predetermined low voltage and a predetermined high voltage;
and further comprising:
a first terminal for applying a voltage potential to the first enclosure; and
a second terminal for applying a voltage potential to the second enclosure.

9. The electronic circuit of claim 8 and further comprising circuitry for connecting the first terminal to the second terminal.

10. The electronic circuit of claim 9 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

11. The electronic circuit of claim 10 and further comprising circuitry for connecting the first terminal and the second terminal to the predetermined low voltage.

12. The electronic circuit of claim 10 and further comprising:
circuitry for connecting the first terminal to the predetermined low voltage; and
circuitry for connecting the second terminal to the predetermined high voltage.

13. The electronic circuit of claim 6:

wherein the first enclosure comprises a transistor collector;

wherein the first well comprises a transistor base;

and further comprising a transistor emitter formed as a region within the first well.

14. The electronic circuit of claim 13 wherein the transistor comprises a vertical PNP transistor.

15. The electronic circuit of claim 14:

wherein the transistor collector is operable in response to an operating voltage that may swing between a predetermined low voltage and a predetermined high voltage;

and further comprising a terminal for applying a voltage potential to the second enclosure.

16. The electronic circuit of claim 15 and further comprising circuitry for connecting the terminal to the predetermined high voltage.

17. The electronic circuit of claim 4:

wherein the first well comprises circuitry operable to emit electrical holes in response to an operating voltage that may swing between a predetermined low voltage and a predetermined high voltage;

and further comprising:

a first terminal for applying a voltage potential to the first enclosure; and

a second terminal for applying a voltage potential to the second enclosure.

18. The electronic circuit of claim 17 and further comprising circuitry for connecting the first terminal to the second terminal.

19. The electronic circuit of claim 18:

wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type;

and further comprising circuitry for connecting the first terminal and the second terminal to the predetermined low voltage.

20. The electronic circuit of claim 18:

wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type;

and further comprising:

circuitry for connecting the first terminal to the predetermined low voltage; and

circuitry for connecting the second terminal to the predetermined high voltage.

21. The electronic circuit of claim 4:

wherein the first enclosure comprises a transistor collector;

wherein the first well comprises a transistor base;

and further comprising a transistor emitter formed as a region within the first well.

22. A method of forming an electronic circuit, comprising the steps of :

forming a first layer in a fixed physical relation to a semiconductor substrate;

forming a well formed in the first layer, wherein the well comprises a first conductivity type and has a side dimension and a bottom dimension;

forming a first enclosure surrounding the side dimension and the bottom dimension of the well, wherein the first enclosure comprises a second conductivity type complementary of the first conductivity type and has a side dimension and a bottom dimension; and

forming a second enclosure surrounding the side dimension and the bottom dimension of the first enclosure, wherein the second enclosure comprises the first conductivity type.

23. The method of claim 22:

wherein the well comprises a first well; and

wherein the step of forming first enclosure comprises the steps of:

forming a second well surrounding the side dimension of the first well; and

forming a buried layer adjacent the bottom dimension of the first well.

24. The method of claim 23 wherein the step of forming a buried layer occurs prior to the step of forming the well.

25. The method of claim 23 wherein the first conductivity type comprises n-type and wherein the second conductivity type comprises p-type.

26. The method of claim 25 wherein the step of forming a buried layer comprises implanted at a dosage on the order of $5e^{15}/cm^2$ and at an energy on the order of 60 keV.

27. The method of claim 25:

wherein the buried layer comprises a first buried layer; and

wherein the step of forming a second enclosure comprises the steps of:

forming a third well surrounding a side dimension of the second well; and

forming a second buried layer adjacent a bottom dimension of the first buried layer.

28. The method of claim 27 wherein the step of forming a second buried layer comprises implanted at a dosage on the order of $8e^{13}/cm^2$ and at an energy on the order of 60 keV.

29. The method of claim 27 wherein the step of forming a second buried layer occurs prior to the step of forming the third well and prior to the step of forming the second well.

30. The method of claim 22:

wherein the first enclosure comprises a transistor collector;

wherein the first well comprises a transistor base;

and further comprising the step of forming a transistor emitter as a region within the well.

*****